Physics of CdTe Photovoltaics: from Front to Back

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ABSTRACT

We discuss physical mechanisms underlying the performance and stability of CdTe based thin-film PV. The processes in (i) photovoltaic junction, (ii) back contact, (iii) nonuniformities, (iv) grain boundaries, and (v) light-induced degradation are addressed including their interactions. The physics of thin film PV turns out to be quite different from that of crystalline PV. High surface-volume ratio and lack of crystallinity result in strong interfacial effects, lateral nonuniformities, and shunting-like and adhesion instabilities in thin film structures. This paper is aimed at presenting a 'big picture'; also, it suggests practical ways of improving thin-film PV.

1. INTRODUCTION

Device physics has been a key factor in established semiconductor technologies, such as crystalline Si, Ge, and various $A^{III}B^{V}$. However, after more than two decades of extensive research, some features unique to thin-film PV have become apparent that are not readily understood in the existing framework. Such are, for example, variations between the characteristics of nominally identical devices, extremely high sensitivity to minute surface treatments, unusual degradation kinetics, and super-additive effects of independent factors. In general, the film small thickness and non-crystalline structure seem to be the key factors underlying the observed peculiarities of thin-film PV. This manifesto is aimed at presenting our view of physical mechanisms by which these factors determine thin film PV properties.

The paper organized as follows. In Sec. 2 we describe the generic structure and basic parameters of CdTe based solar cells. Sec. 3 gives a phenomenological view of nonuniformities applicable to subsequent topics. In Sec. 4 we consider the physics of the device main junction. Sec. 5 deals with the back contact, another junction that can be highly non-ohmic. Sec. 6 explains interaction between the main junction and back contact. Sec. 7, 8 briefly discuss the role of grain boundaries and recombination. Sec. 9 addresses the physics of degradation. Conclusions are given in Sec. 9.

2. CELL STRUCTURE AND BASIC PARAMETERS

This section contains a compressed introductory compilation of the basic facts from several sources, of which we mention the reviews in [1]. The superstrate structure sketch in Fig. 1a can represent practical devices in a wide range of their constituting layer thickness: 0.1 – 0.3 μm for the conductive transparent oxide (TCO) and buffer layers, 0.08 – 0.3 μm for CdS, 1.5 – 7 μm for CdTe, all deposited on 1 – 3 mm thick glass [1]. $CdCl_2$ treatment and Cu introduced through the back contact are necessary elements of many successful recipes.

The corresponding band diagram (Fig. 1b) shows a one-dimensional view including three conceivable models for the CdS/CdTe conduction band offset. The component forbidden gaps are approximately 2.4 eV for CdS and 1.5 eV for CdTe. In the region of metallurgical junction,

they can form a solid solution with a slightly different optical gap of 1.46 eV. Based on the parameters of standalone CdTe and CdS, the 'main stream' interpretation is that they form a p-n junction. The light is absorbed mostly in the CdTe layer where also the most of built-in field and electric potential reside.

In addition, there is typically a back barrier between the CdTe and back contact metal, whose height varies in the range of ~ 0.3 – 0.8 eV depending on the back contact recipe. It can set a significant obstacle to the photo-generated holes. Different kinds of doping and surface treatments are used to increase its transparency. A possible front contact barrier (spike), if exists, cannot be significant, not exceeding the back barrier, say, less than ~ 0.5 eV in order to avoid the photocurrent blocking.

The curvature of the diagram in Fig. 1b is determined by the space charge density n, generally different in CdS and CdTe. A related screening (depletion) length $L = \sqrt{\kappa V_{BI} / 2\pi e N}$ in working devices is estimated as $L_{\mathrm{CdTe}} \sim 1-3\ \mu m$, corresponding to the acceptor concentration of N_{CdTe}~10^{13}-10^{14} cm^{-3}, dielectric constant $\kappa \sim 10$, and the barrier (built-in voltage) of V_{BI}~ 1V.

The curvature is known with much less certainty for the case of CdS. As grown this material has the electron concentration $N_{\mathrm{CdS}} \sim 10^{18}$ cm^{-3} and $L_{\mathrm{CdS}} \sim \left(N_{CdTe} / N_{CdS}\right) L_{CdTe} << L_{CdTe}$. Because it cannot be less than the average distance between the screening charges, we put $L_{\mathrm{CdS}} \sim 0.01\ \mu m$. On the other hand, there is ample evidence of CdS becoming strongly depleted in the cell structure where, in particular, it accumulates compensating Cu defects [2]. A depleted CdS will have much greater screening length, $L_{\mathrm{CdS}} \geq 1\ \mu m$ exceeding its thickness. In the latter case, CdS behaves as an insulator between a metal TCO and p-type CdTe; correspondingly, the entire structure becomes an MIS type PV rather than a p-n junction (see Sec. 4 below).

Under 1 sun illumination and room temperature, the typical photovoltaic parameters of CdS/CdTe devices are: open-circuit voltage Voc~0.8V, short-circuit current density Jsc~20mA/cm^2, fill-factor FF~60-70%, series resistance typically not exceeding several Ω-cm^2, TCO sheet resistance ρ~10 Ω/□, and nowadays routinely obtained efficiencies in the range of 10-13% for cells of 1 cm or less in diameter.

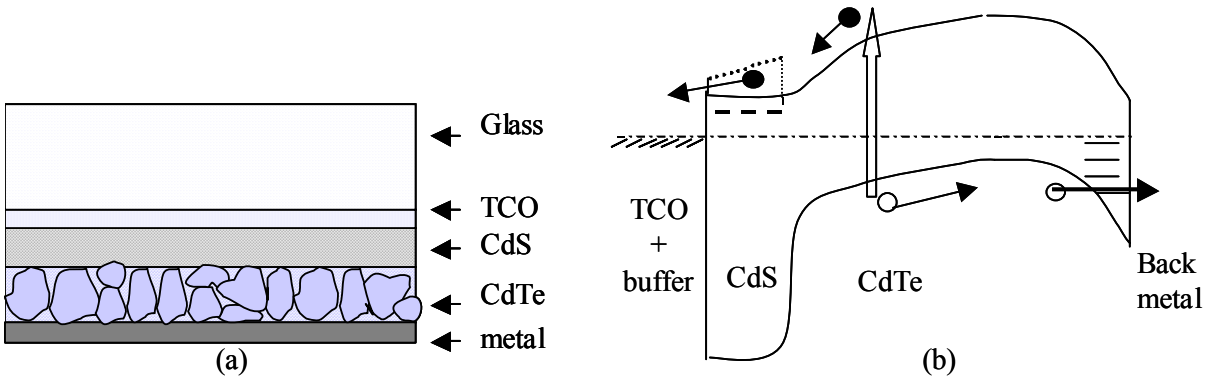


Figure 1. (a) CdS/CdTe solar cell structure (not to scale). The polycrystalline structure of CdTe film is schematically shown. (b) In the corresponding band diagram, solid line represents the model of zero band offset between CdS and CdTe, while the dashed and dotted lines illustrate the models of cliff and spike offsets respectively. Fat arrow shows the electron-hole pair generation. Solid arrows illustrate the electron and hole transport including barrier penetration by activation and tunneling.

3. LATERAL NONUNIFORMITIES

In a polycrystalline thin-film device containing not too many grains across its thickness (Fig. 1a), lack of self-averaging results in lateral variations between different spots. It is natural to represent these spots by random micro-diodes forming random diode arrays. At the cell level, random diodes are connected in parallel through a resistive TCO electrode (Fig. 2a); however, the random diode circuitry becomes more complex at the level of integrated large-area module. Lateral nonuniformities in thin-film PV have been detected by many different techniques, such as STM, optical beam induced current, electron beam induced current, electrical mapping, photoluminescence, electroluminescence, and thermography (see [3,4] and references therein).

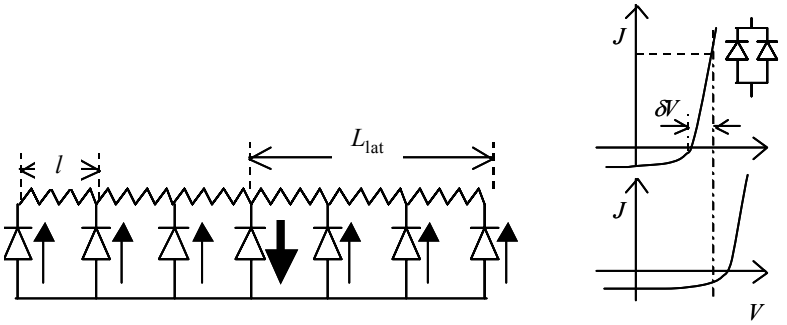
Weak (low Voc) diodes are most detrimental: under forward bias generated by their neighbors, they run currents in the 'wrong' direction, and shunt the device. On experimental grounds, it is believed that a typical thin-film system contains a variety of weak diodes with continuously distributed Voc. The distribution consists of a Gaussian-like peak superimposed on a low-value tail extending to the range of Voc several times smaller than the average.

Weak diode effects span macroscopically large distances,

$$L_{\text{lat}} = \left(\Delta V / \rho J_{sc}\right)^{1/2}, \quad \Delta V = \max\left\{kT/q; \delta V\right\} \tag{1}$$

where kT is the thermal energy, q is the electron charge, and δV is the difference between the electric potential across the shunt (weak diode) and that of across the device far from the shunt. In brief, L is estimated from the condition that the resistive voltage drop across the cell balances the original potential difference ΔV (see [3] for detail). Even the minimum screening length L_{lat} (with $\Delta V=kT/q$) is macroscopically large, of the order of 1 mm at room temperature under 1 sun illumination. It is still larger, approaching several centimeters for a dead shunt ($\Delta V=Voc$) or sufficiently weak diode ($Voc>\Delta V>>kT/q$).

It is clear from Fig. 2b that the total current robbed by a weak diode strongly depends on the steepness of the J-V curve in the first quadrant. Note in this connection that a series resistance (not shown in Fig. 2a) will change the weak diode J-V curve from exponential to linear for V



(a) (b)

Figure 2. (a) Random diode array representing a laterally nonuniform solar cell. Fat arrow shows strong recombination current through a weak diode that robs potentially useful currents generated by its more robust neighbors in the region L. (b) J-V characteristics representing a weak diode (top) and its neighborhood (bottom).

considerably greater than *Voc*. Therefore, one can expect a back barrier or other series resistance source to suppress the nonuniformity related effects [3,5]. In fact, the situation is more complex: we will see in Sec. 6 that the back barrier can make J-V curves steeper.

A system of many interacting random micro-diodes ($l << L_{\text{lat}}$ in Fig. 2a) can exist either in almost uniform or strongly nonuniform state and the transition between these states occurs at a critical value of a dimensionless parameter characterizing the disorder [6]. This parameter becomes bias dependent under external voltage. As a result, the system undergoes the transition into the nonuniform state above certain voltage Vc (> Voc) that depends on the system disorder [7]. One manifestation of this transition is that J-V, curves of nominally identical cells are very close when V<Vc; however, they appear significantly different (fan) when V>Vc.

Voltage dependent collection [8] is another effect observed in thin film PV and attributable to weak diodes. Indeed, under open-circuit conditions, the weak diodes will consume all the photogenerated current. As the voltage decreases below Voc, it becomes clear from Fig. 2b that weak diodes consume less photocurrent; hence the charge carrier collection increases.

By extensive modeling, it was established that of all local parameters, Voc fluctuations are most significant [3]. It is not unusual for thin film cells of sub-centimeter size to have distribution of Voc dispersed in the range of 5 to 15%, which results in the cell efficiency loss estimated as ~10-15%. Furthermore, at the integrated module level, the nonuniformity effects are additionally promoted by highly conductive cell interconnects [9]. This can explain the observed broad distributions of integral parameters of the nominally identical PV modules [10]. Our rough estimate of the nonuniformity loss in large area thin film modules is 20-30%.

Physical sources of Voc fluctuations include nonuniformities in the main junction and back barrier (Sec. 4-6). Depending on their nature, the space scale of lateral fluctuations (l in Fig. 2a) can vary from a micron scale (grains) to millimeters (wet treatments) and meters (deposition nonuniformity). Regions separated by distances larger than L_{lat} are electrically disconnected. In particular, $L_{\text{lat}} \sim \left(V_{oc}/\rho J_{sc}\right)^{1/2} \sim 1\,\text{cm}$ determines the maximum linear dimension of a cell in which all the sub-areas contribute to the power output; in larger cells some regions are blocked.

The above understanding has suggested a successful approach to blocking nonuniformity by applying 'self-healing' electrolyte treatments [11]. These treatments create interfacial layers between the CdTe and back metal, which increases the cell efficiency; curiously, red wine was the first such discovered treatment [12].

4. MAIN JUNCTION

While the standard interpretation treats CdTe/CdS as a p-n junction (Figs. 1b and 3b) [13], some recent data suggest that CdS/CdTe PV operates rather as a MIS structure sketched in Fig. 3c [14]. The main observation behind the MIS model is that of the buffer layer effect, namely, causing high Voc.

Indeed, Table I shows that the standard Cu doping becomes unnecessary when a proper buffer layer is used between the TCO and CdS. This means that the structure of the metal part of the device affects the parameters of the main junction CdS/CdTe. Such a reach-through interaction seems surprising in the light of the above-mentioned (Sec. 2) high charge density and small screening length L in CdS: no interaction through CdS would be allowed when $L << l$.

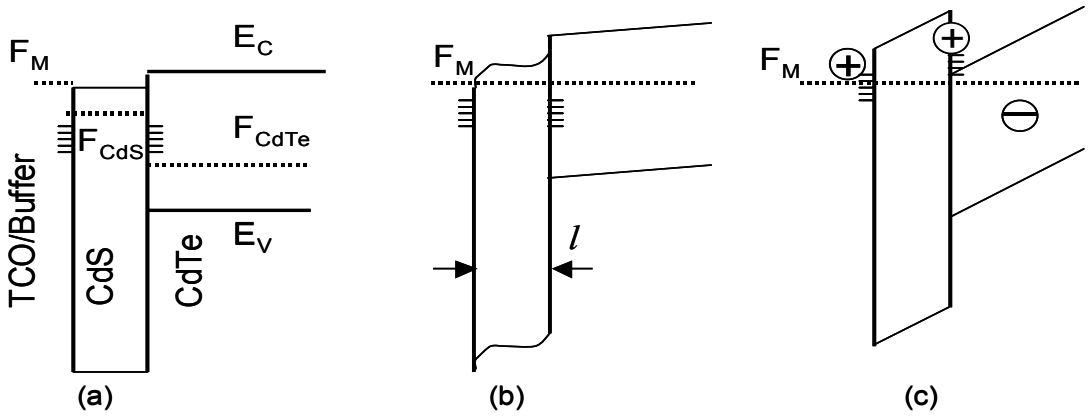


Figure 3. Towards MIS band diagram of CdS/CdTe photovoltaics (not to scale). (a) Band diagrams and Fermi levels (F) of the three components before they interact: metal (representing TCO or TCO coupled with buffer), CdS layer, and much thicker CdTe (not to scale). (b) p-n junction band diagram due to interaction between the components when the CdS thickness is larger than its screening length, $l>>L$. (c) The MIS composite band diagram for the case of $l<<L$; the barrier shape depends on the electric charge distribution and can be different. + and - show the electric charge distributions. Also, shown in the diagrams are the interfacial states.

Table I. PV parameters of CdTe thin-film cells with and without intentional Cu and buffer layer.

Cu and buffer Recipe	**Cu doped**	**No Cu**
Buffer layer present	Voc~0.8V, Eff ~ 12%	Voc~0.8V, Eff ~ 12%
No buffer	Voc~0.8V, Eff ~ 12%	Voc~0.4V, Eff ~ 4%

To explain these observations we assume that the originally conductive CdS gets strongly compensated as imbedded in the device structure, and behaves there as an insulator ($L>>l$). This suppresses the Schottky barriers between CdS and its tangent layers, and couples the metal part of the device with the CdTe; hence strong bending of CdTe bands and high Voc (Fig. 3c). The concomitant CdS barrier for the electrons is transparent via defect assisted tunneling.

According to our understanding, the CdS compensation can be achieved through either doping (Cu accumulation in CdS [2]) or by creating surface states as a result of interaction with the buffer layer (lattice mismatch may be essential). In other words, doping and surface modification have the same effect. Such a strong surface effect becomes possible because CdS layer is thin and does not have enough bulk to balance surface states. Note that the buffer layer concept originally introduced to reflect decoupling, is reversed here: our "buffer" effectively couples the metal and semiconductor layers. The above mechanism of MIS junction and buffer layer effect can be common between the CdTe and CIGS PV.

Consistent with the MIS model are observations of highly resistive CdS in efficient CdTe PV. It has been established that adding Cu leads to significant depletion of CdS, which testifies against the p-n junction model of CdTe PV [15]. Similarly indicative are recently developed highly resistive CdS:O layers in CdTe PV [16].

Practically speaking, the MIS model suggests that doping may not be a necessary part of a successful recipe, and one can prepare the desired highly resistive CdS by changing its surface, for example, properly choosing a buffer layer or deposition techniques or parameters. Indeed, in some cases tuning the deposition parameters has led to high Voc devices without Cu and without

buffer layer. Similarly, with the originally resistive CdS, such as the chemical bath deposited CdS, neither the buffer layer, no Cu may be needed to make a high-Voc device [17].

In implementing Cu-free main junctions, care should be taken not to wash out other useful Cu related effects, such as, for example, Cu doping of the back contact (see Sec. 5). Another potentially masking effect is related to the buffer layer. Being capable of clogging shunts, the buffer layer may appear beneficial even when it is not needed for making highly resistive CdS.

One other reading of the MIS model is that while Cu makes the CdS resistive, it may not be that important for the CdTe doping (suggested in some models of CdTe PV to explain the positive Cu effect). Indeed, it was recently observed that adding Cu directly to CdS prior to CdTe deposition makes an efficient PV device [18].

In conclusion we note that while Cu in CdS can be beneficial due to its induced depletion, it can also lead to detrimental effects when used in too high concentrations. Namely, it can form conductive paths through the CdS thus locally shorting the device, in other words, creating weak micro-diodes. This is consistent with the observations in [18] and with the increase in device nonuniformity after light soak [4,19]. [Missed CdS grains (pinholes) can be another significant source of the main junction nonuniformity.]

5. BACK CONTACT

Back contact recipe has a profound effect on CdTe PV parameters, in particular, on device Voc. This effect has been somewhat mysterious because a typical back contact is optically inactive and thus cannot generate photovoltage; we suggest an explanation in Sec. 6 below. The nature of back contact effects is attributed to its Schottky barrier, which acts as a diode in the "wrong" direction, opposite to the main junction. This phenomenon also known as the back barrier or back diode, or back surface field can affect all major PV.

Doping is a known method of suppressing the back barrier. In the case of CdTe PV, Cu doping is beneficial. Such doping can act through: (1) decreasing the barrier width by adding to the space charge density and thus shrinking the screening length L_{CdTe} near the back contact, and (2) creating defect states that allow hopping transport through the barrier.

A common equivalent circuit for the back barrier is a back diode in series with the main junction photo-diode. One result of such modeling is a rollover in the first J-V quadrant shown in

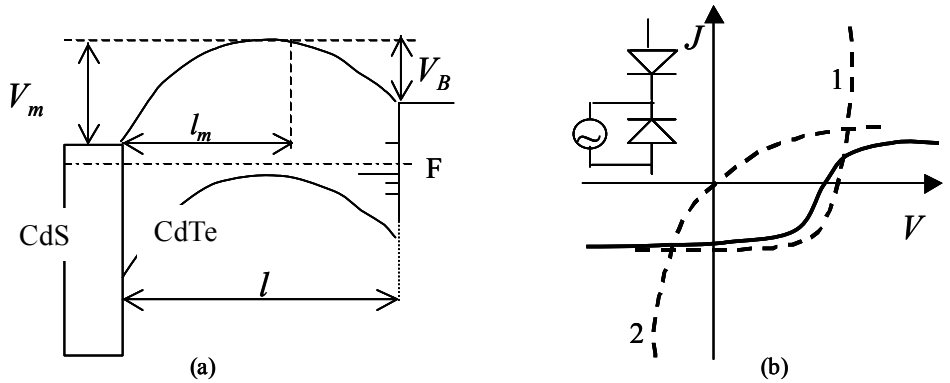


Figure 4. (a) Generic band diagram of CdTe thin-film PV (details of the main junction neglected) containing a back barrier with defect levels in it. (b) Its J-V characteristics composed of the main junction (1) and back diode (2) J-V curves in accordance with the equivalent circuit in the inset.

Fig. 4b. In many cases the observed J-V rollovers vary between nominally identical cells. This is most likely related to the random nature of the barrier as explained below.

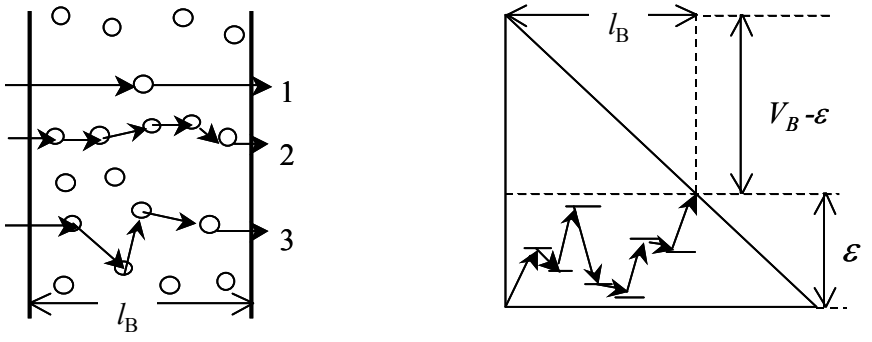
Two extreme mechanisms for the back barrier transparency are activation and tunneling, with the probabilities $\exp(-V_B/kT)$ and $\exp(-2l_B/a)$ for the high and low temperature regimes respectively, where a is a properly defined decay scale for the electron wave function under the barrier. At the first glance, tunneling is unlikely for the typical T~300K, V_B~0.5 eV, $l_B \sim 0.1$ μm, and a~10Å. However, defect states in the barrier region permit tunneling (hopping) across distances much smaller than l_B, hence, with exponentially higher probability $\propto \exp(-2l_B/Na)$, where N is the number of participating defects. Therefore defect chains form efficient pathways through the barrier (Fig. 5). Such defect-assisted transport has much in common with the transversal hopping conduction through amorphous thin films [20]. Along the same lines, the pathway resistance exponentially decreases with N, while the probability $p^N = \exp[-N\ln(1/p)]$ to find an N-defect pathway exponentially decreases. The most efficient pathways optimizing between these trends contain the number of defects

$$N \approx \sqrt{l_B/a\Lambda} >> 1 \text{ with } \Lambda = \ln(1/p) \approx \ln(1/ga^3kT) >> 1 \qquad (2)$$

where g is the defect density of states ($cm^{-3}eV^{-1}$). Note that other pathways contain different numbers of defects and have exponentially different (generally, non-ohmic) resistances.

Spatial inhomogeneities in barrier doping serve as another source of lateral nonuniformity. This was discussed by Tung [21] in the classical approximation where the local barrier height remains the only random parameter. Strong ($>>kT$) fluctuations in the Schottky barrier height have been observed even for metals deposited on crystal surfaces [22]; stronger effects can therefore be expected for the case of rough surface such as that of polycrystalline CdTe.

We conclude that the back barrier transparency fluctuates in the lateral directions. The corresponding exponentially dispersed resistances are connected in series with random diodes representing the device main junction. A low Voc micro- diode in series with an abnormally transparent back barrier spot gives a 'dangerous' weak diode (shown in Fig. 2b) that can effectively shunt the device. This suggests a conceivable explanation of how an optically inactive back contact can affect the device Voc.



(a) (b)

Figure 5. (a) Electron hopping through a barrier in the real space; open circles represent defects. Pathways 1, 2, and 3 correspond to the regions of abnormally low, high, and average transparency respectively. (b) Hopping through a triangular barrier in the energy space including thermal activation in the energy band ε; cf. the back barrier triangular shape in Fig. 1b.

6. INTERACTION BETWEEN FRONT AND BACK JUNCTIONS

Experimentally, Voc suffers the most when the back barrier is strong [23]. As explained next, the low transparency spots in the back barrier are most detrimental due to their interactions with the main junction.

We start with noting that the back diode concept implies no space charge accumulation, hence, a barrier low enough to let a charge carrier (hole in the case of Fig. 6a) leave the device before another carrier is generated nearby. When the back barrier grows above certain value, it blocks the holes and the device supplies no current even under short-circuit conditions. Instead, the photo-generated electron hole pairs recombine as illustrated in Fig. 6b. Applying a forward bias above a threshold value $V>V_{RT}$, turns the device into the reach-through regime where the forward current is not blocked by the main junction barrier. It then flows freely provided that the window layer is transparent enough (Fig. 6c), which we assume here. The corresponding J-V curve (Fig. 6d) will have a threshold voltage V_{RT}, which depends on the device built-in potentials V_m and V_B (Fig. 4a), in a simple approximation $V_{RT} \approx 2V_m\left(1-\sqrt{V_B/V_m}\right)$ [23]. Thus either locally weak main junction (Sec. 4) or low transparent back barrier (Sec.5) can lead to low local V_{RT}, i. e. reach-through micro-diodes.

At the first glance, it is counterintuitive that local spots of low back barrier transparency significantly decrease the system Voc, for the current should flow round such spots making their presence immaterial. However, exactly because of the photocurrent flowing around, such spots find themselves under significant forward bias where they become nonlinear shunts and decrease the system Voc.

Remarkably, no series resistance is associated with reach-through micro-diodes, as can be concluded from Fig. 6; hence they appear to be the most efficient shunting entities. This prediction has been verified experimentally [23]: no evidence of series resistance was detected up to J of the order of several hundred of mA/cm^2.

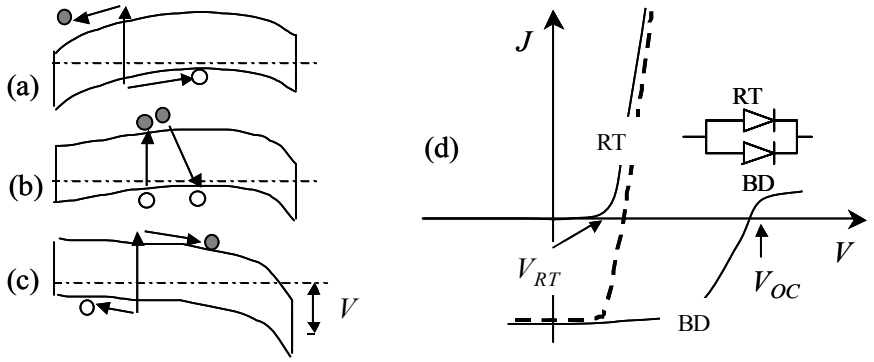


Figure 6. (a) CdTe layer with relatively low back barrier operating in the back diode regime. (b) Back barrier blocked CdTe under short-circuit. (c) Same under reach-through conditions, $V>V_{RT}$. Arrows show the electron-hole generation and subsequent transport. (d) J-V characteristics of the standard back-diode (BD, with rollover) and reach-through (with a lift off at V_{RT}) devices. The dashed line corresponds to a combination of the standard and reach-through parts in parallel where V_{RT} appears to play the role of the open-circuit voltage Voc.

Because shunting by reach-through micro-diodes is similar to that by weak diodes (Sec.2), all the results of the weak diode theory can be extended to the case of reach-through micro-diodes, including that of the screening length, decrease in device Voc, phase transitions between small and strong fluctuation regimes, bias dependent collection, and others. Overall, the concept of reach-through micro-diode reveals a mechanism of strong interaction between the main junction and back contact where their properties appear non-additive.

7. GRAIN BOUNDARY EFFECTS

The question of grain boundary (GB) effects attracted a considerable attention in the recent years. GB are considered beneficial to device performance because their built-in electric fields spatially separate electrons and holes thereby suppressing their recombination. While suggested only recently for CdTe PV by Kaydanov and others [24], this mechanism (Fig.7) was developed much earlier for other polycrystalline materials showing high photoconductivity [25].

One subtlety illustrated in Fig. 7c is that the electric potential along GB must be nonuniform to keep the electrons and holes apart when the latter cross GB [25]. Such nonuniformity naturally appears with spatial fluctuations in the density of the electric charge trapped by GB defect states.

Another important point is that while beneficial as a source of potential barrier [26], defects in GB can promote the electron-hole recombination. Some GB passivation, say, through $CdCl_2$ treatment or Cu doping may be required to block this effect. The required passivation seems to have been achieved in the existing recipes with the internal quantum efficiency, QE >90%.

In conclusion, GB act as effective circuitry separating the electrons from holes and delivering them to external contacts without recombination. It is rather due to those conductive contacts that electrons can use the device nonuniformities finding their ways back to the holes thereby hurting the device performance.

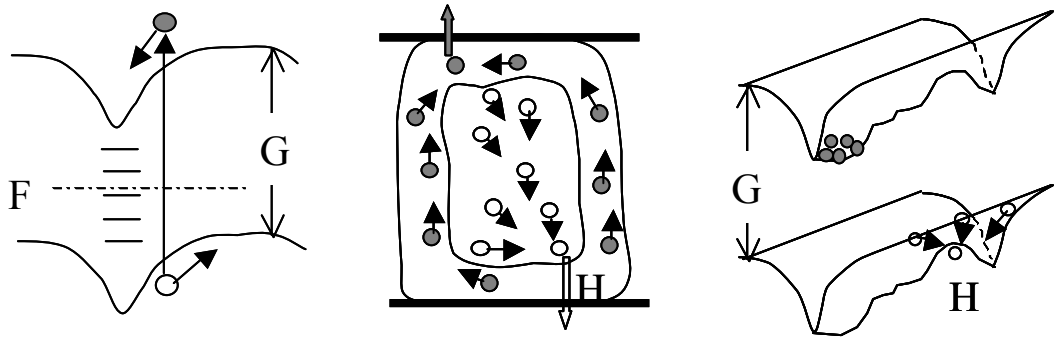


Figure 7. (a) GB band diagram showing the electric field that spatially separates electrons and holes moving them into GB and internal grain region respectively; F is the Fermi level, G is the forbidden gap. Short horizontal lines represent defect states. (b) The electron current is contained in GB region connected to the contacts (solid lines) that can represent either external metal or other grains. The hole current crosses GB at a point (H) where GB barrier is a minimum for holes and a maximum for electrons. (c) Vicinity of the same point H in the energy space: electrons and holes are spatially separated.

8. IRRELEVANCE OF RECOMBINATION AND SPECIFICITY OF THIN-FILM PV

Consistently high QE in many different recipes testify against the recombination time τ_r as a relevant thin-film PV parameter. Assuming the opposite would imply τ_r comparable to the drift time τ_d. Because of completely different physics behind these two, the relationship $\tau_r \sim \tau_d$ would be unlikely coincidence. Instead, either $\tau_r << \tau_d$ or $\tau_r >> \tau_d$ should take place. The latter should be chosen (i) on empirical grounds, (ii) because τ_d is rather short (in nanosecond range) for thin-film PV, and (iii) recombination is suppresses by the grain boundary effects. This choice makes recombination irrelevant.

The observed small deviations of QE from 100% should be attributed then to the *spatially nonuniform* (forced) recombination through weak diodes or other shunting entities, in which electrons and holes are pushed towards each other. Therefore, nonuniformity related weak elements and contacts through which they act, become especially sensitive elements of thin-film PV technology, generally consistent with observations.

The physics can be different for crystalline PV where (1) in the absence of grain boundary effects, electrons and holes are not spatially separated and recombine uniformly, and (2) larger thickness makes the drift time much τ_d longer, possibly somewhat comparable to τ_r.

9. DEGRADATION MECHANISMS

All kinds of PV somewhat degrade under light soak. Here is a summary of significant observations for CdTe based PV. (1) Degradation rates can depend on details of device recipe; they can vary between nominally identical samples. (2) Extremely stable CdTe devices are occasionally reported. (3) Voc and FF drop are most typical modes of degradation. (4) Degradation rate is higher under open-circuit compared to short-circuit and optimum power conditions. (5) It generally increases with T [27]. (6) Shunting can be responsible for significant part of degradation. [28]. (7) Lateral nonuniformity increases with degradation [4,19].

We reduce the existing hypotheses on the underlying mechanisms to just four, simplistically explained as follows.

(a) *Defect generation*. Via e-h recombination or trapping, light generates defects, which promote recombination (another wording is that defects shift quasi-Fermi levels). This mechanism alone is hard to reconcile with the above facts (1) and (2). However, it might contribute to (b) and (c) below.

(b) *Electromigration*. Light induced changes in the defect charge states trigger their migration in the device electric field; Cu diffusion is discussed the most (following Kaydanov). This is consistent with the understanding that removal of Cu makes back contact less transparent for holes resulting in reach-through micro-diode shunting (Sec. 6) and related drop in Voc and FF. In addition, it promotes Cu accumulation and shunting in CdS (Sec. 4), again hitting Voc and FF. Because diffusion is sensitive to the temperature and material, this mechanism agrees with all the above facts.

(c) *Shunting-like instabilities*. Stresses concentrate on weak spots causing their additional degradation. This may occur through dendrite growth [28] or precursor defect chains [29] similar to that described in Sec. 5. Small film thickness increases the shunting probability. This mechanism can partially utilize (a) and (b), and generally agrees with the observations.

(d) *Metal delamination*. Through bias dependent adhesion between back metal and semiconductor, lateral nonuniformity in the electric potential translates into tangential

stresses and delamination spots conducive to electric breakdown [27]. Even before the breakdown, the delamination spots act as reach-through diodes; hence, decrease in Voc and FF. This mechanism is consistent with the above observations and with long-standing folklore of delamination related problems.

This section is hard to conclude, partially because the degradation issues are sensitive and corresponding data are rarely published. We restrict ourselves to asserting that major degradation facts fit the above-outlined physics of lateral nonuniformities, exponentially varying barrier transport, and strong interaction between the front and back contacts. The presence of metal contacts appears essential to all of the above mechanisms except (a). Therefore, it is rather a device structure and not its component material that dominates the observed degradation.

10. CONCLUSIONS

In conclusion, the physics of thin-film CdTe PV is quite different from that of crystalline devices. Here is the concept summary:

- CdTe based PV is a MIS (rather than p-n) type of device where the CdS depletion can be achieved by Cu doping or, alternatively, via defect states introduced by a buffer layer.
- Back contact electronic transparency varies exponentially in the lateral directions combining spots of extremely low and high series resistance.
- The device main junction and back contact interact forming local elements ranging from photo-diodes with random Voc and series resistance to random reach-through diodes.
- Weak micro-diodes and reach-through diodes effectively shunt the device thereby decreasing its Voc and FF; their shunting abilities are random and voltage-dependent.
- The effects of local nonuniformities of any kind (shunts, weak diodes, reach-through diodes) span macroscopic distances of a millimeter or larger scale.
- Grain boundaries play a positive role separating the electrons from holes. It is essential for this function that the electric potential varies along grain boundaries.
- The recombination time seems to be irrelevant as a physics parameter for thin-film PV.
- The observed degradation can be understood within the above framework combining lateral nonuniformities, barrier transport, shunting, and interacting device junctions.

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